IN THE CLAIMS

Please cancel Claims 8-10, 12, and 20-21 without prejudice and amend Claim 22 and 24 as shown in marked-up form as follows:

1. (Previously Presented) A data processing system which is adapted to function in a reduced-power mode, comprising:

a first data processing unit that has access to a memory belonging to the first data processing unit: and,

a second data processing unit having its own memory, said second data processing unit having access to the memory belonging to the first data processing unit, wherein the first data processing unit is arranged for offering the second data processing access to the memory belonging to the first data processing unit in a reduce-power mode of the data processing system so that the second data processing unit utilizes the memory belonging to the first data processing unit instead of its own switched-off memory.

2. (Previously Presented) The data processing system as claimed in Claim 1, wherein the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a period of time in which the reduced-power mode of the data processing system implies a reduced-power mode of the first data processing unit.

3. (Previously Presented) A data processing system situated in a reduced-power mode, comprising:

a first data processing unit that has access to a memory belonging to the first data processing unit, wherein the first data processing unit is arranged for offering a second data processing unit access to the memory belonging to the first data processing

unit, and wherein the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit when a memory belonging to the second data processing unit is switched off.

4. (Previously Presented) The system as claimed in Claim 1, wherein the memory belonging to the first data processing unit forms part of the first data processing unit.

5. (Previously Presented) The system as claimed in Claim 1, wherein the memory belonging to the first data processing unit is a cache memory.

6. (Previously Presented) The system as claimed in Claim 1, wherein the first data processing unit is a microprocessor.

7. (Previously Presented) The system as claimed in Claim 1, wherein the second data processing unit is a video controller.

8-10 (Cancelled)

11. (Previously Presented) A data processing unit having access to a memory belonging to the data processing unit that may be situated in a reduced-power mode,

a mechanism that allows the first data processing unit to offer a second data processing unit access to the memory belonging to the first data processing unit in the reduce-power mode, wherein the first processing unit is arranged for offering the second data processing unit access to the first memory when the second memory is switched off.

12. (Cancelled)

13. (Previously Presented) A data processing system that may be situated in a reduced-power mode having a first data processing unit that has access to a first memory

associated with the first data processing unit and a second data processing unit that has access to the first memory, said system comprising:

a second memory operating in a switched-off state associated with the second data processing unit; and

a mechanism that allows the first data processing to offer the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system so that the second data processing unit does not access the second memory during reduced power mode when the first memory can service the second data processing unit.

14. (Previously Presented) The data processing system as claimed in Claim 13, wherein the second memory unit can be accessed by system components other that the first or second data processing units in the reduced-power mode.

15. (Previously Presented) A data processing system which may be situated in a reduced-power mode having a first data processing unit that has access to a first memory associated with the first data processing unit and a second data processing unit that has access to the first memory comprising:

a second memory associated with the second data processing unit; and

a mechanism that allows the first data processing unit to offer the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system, wherein the first data processing unit is arranged for offering the second data processing unit access to the first memory when the second memory is switched off.

16. (Previously Presented) The system as claimed in Claim 15 wherein the memory belonging to the first data processing unit forms part of the first data processing unit.

17. (Previously Presented) The system as claimed in Claim 15, wherein the memory belonging to the first data processing unit is a cache memory.

18. (Previously Presented) The system as claimed in Claim 15, wherein the first data processing unit is a microprocessor.

19. (Previously Presented) The system as claimed in Claim 15, wherein the second data processing unit is a video controller.

20-21 (Cancelled)

22. (Previously Presented) ~~The~~ A data processing configuration comprising:

a first processor in communication with a memory, the first processor operating in a reduced-power mode and accessing a selected portion of a first memory; and

a video controller arranged to access unselected portions of the first memory belonging to the first processor, the video controller further assessing a second memory associated with the video controller~~as claimed in claim 20~~, wherein the video controller is inhibited from accessing the second memory.

23. (Previously Presented) The data processing configuration as claimed in claim 22, wherein the video controller is disconnected from the second memory.

24. (Currently Amended) The data processing configuration as claimed in claim 22, wherein an energy supply to ~~the~~ a video controller memory is interrupted.